8.1.1 Transmit Oscillator Assembly

8.1.1.1 Description

The transmit oscillator supplies approximately +29.5 dBm of peak pulse power at a fixed frequency of 5.8 GHZ. To conserve average D.C. power consumption, it is gated through the duty factor board by a TTL input signal. The maximum turn-off/turn-on delay times are 100 ns.

For signaling purposes, the transmit oscillator is amplitude modulated by -1 dB through the duty factor board by a CMOS input signal.

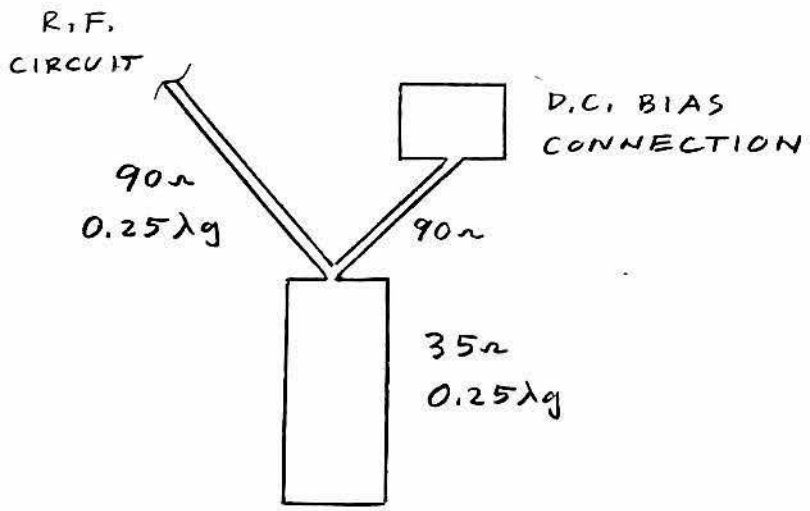
8.1.1.2 Design Requirements

1. Peak pulsed output power of +28 dBm with a 330 nsec pulse at a repetition frequency of 44 KHz to 81 KHz.
2. Frequency of 5.8 GHz.
3. Maximum turn-on and turn-off delay times of 100ns with a TTL input signal.
4. Capability of being amplitude modulated by -1dB, with good temperature stability, by a CMOS input signal.
5. Power supply voltages of +5 VDC and -10 VDC were available.
6. Minimize DC power consumption.
7. Stable 5.8 GHz oscillation with an all phase isolator load.
8. Low R.F. leakage through case.

8.1.1.3 Design Procedure

Thin film alumina substrates were utilized for the power oscillator because of the high frequency of operation, 5.8 GHz. Without wrap around grounds, good thin film R.F. grounds are difficult to obtain at this frequency. "Via" holes have considerable inductive reactance at 5.8 GHz. Even if compensated by the rest of the circuit, it would be difficult to trim and maintain consistency in production.

Therefore a resonant choke assembly was chosen to provide D.C. bias. A single section resonant choke assembly is shown in Figure 1.



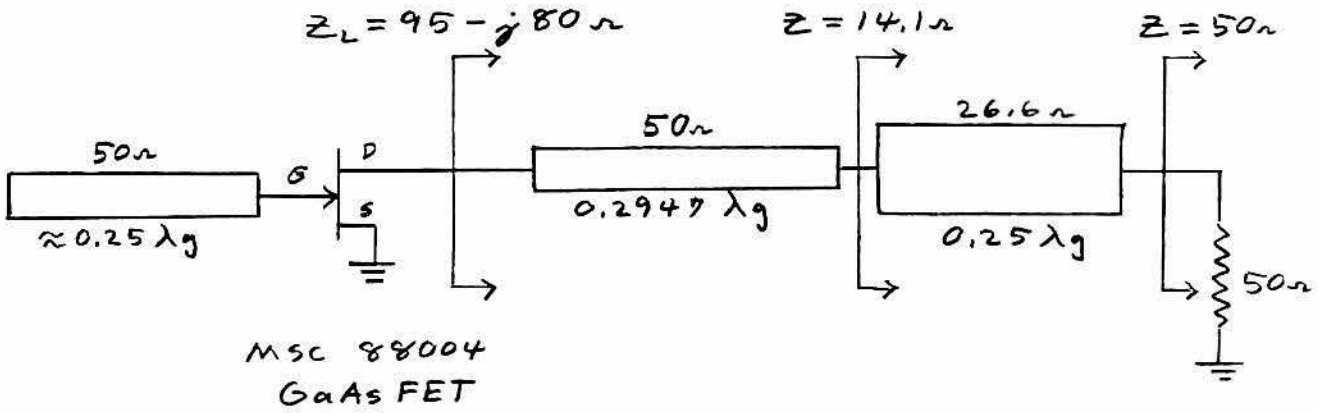
Single Section Resonant Choke Assembly
Figure 1

The minimum line width practical with the thin film process used here is 5 mils. This limits the impedance of the quarter wave series section to 90 ohms. A quarter wave shunt section was selected to be 35 ohms to guarantee operation as a transmission line instead of as a capacitor. This enabled a lower impedance to be obtained at a well defined location. A double section choke assembly was actually used in the oscillator for better isolation.

One disadvantage of using resonant bias choke assemblies is their out of band resonances. The oscillator, when first constructed, produced a dominant spurious response at 1.9 GHz which was not affected by output matching. Thus a load-pull measurement could not be conducted. The double section resonant bias choke assembly and asociated wiring were found to be producing an impedance minima at this frequency as well as many others. The device oscillated at the lowest frequency at which a gate impedance minima could be found, in this case 1.9 GHz. The minimum impedance seen at the gate from the choke assembly was raised to 50 ohms by inserting a 50 ohm chip resister at the gate in series with the first 90 ohm series section of the bias network. This enabled the much lower impedance of the 1/4 λg open circuit tuning stub at 5.8 GHz to become dominant and thereby permitted stable operation independent of the output match.

Small signal S-parameters, provided by MSC at the operating bias levels, were found to be greatly misleading in calculating the required load impedance. The small signal predicted optimum load impedance was 5.75 ohms. After the oscillator was stabilized and a load-pull conducted, the actual optimum load impedance (confirmed by actual circuit layout results) was 95-j80 ohms. In the MSC application note TE-213, their design example at 8 GHz indicated a small signal design load impedance of 15-j40 ohms. Their load-pull showed an actual optimum load impedance of 66-j16 ohms. Note the radical differences between predicted results and actual results. Small signal s-parameters were also found to be misleading when used for in analysis of spurious oscillation modes. This approach was therefore abandoned.

Load-pull measurements with a low-loss double-slug dielectric tuner were conducted at cw to find the correct device load impedance for maximum power output. It was found to be equal to 95-j80 ohms. The simplest series tuned output match that appeared practical is shown in Figure 2 as well as on the Smith chart of Figure 3.



Reverse Channel Oscillator Matching
Figure 2

To obtain the desired load impedance of 95-j 80 ohms the 50 ohm output load impedance is first transformed to 14.1 ohms by use of a quarter-wave transformer. A 0.2947λg length of 50 ohm transmission line is then used to achieve the desired load impedance. A schematic diagram of the complete hybrid micocircuit is shown in Figure 4. Note that the bias choke assemblies are connected to the lowest impedance points of both the gate stub and the drain matching circuit. This minimizes loading effects caused by the bias choke assemblies on the matching circuits and permits greater bandwidth and reproduceability.

Trim pads are provided along the outside of the 26.6 ohm line to increase the width or length as needed for best power output. A diamond scribe may be used to decrease either dimension. On several units, trimming was not required. Actual HMC substrate layouts are given in Figures 5 and 6.

The oscillator duty factor printed wiring assembly interfaces the oscillator HMC bias lines to the outside world. The schematic of the duty factor board is shown in Figure 7. It establishes the correct operating bias current, gates the oscillator on and off by the "Transmit Duty Factor" TTL input, as well as providing A -1dB amplitude modulation controlled by the "Modulation" CMOS input.

The MSC 88004 device is operated reverse channel to provide an internal R.F. feedback mechanism, which deletes the requirement for an external R.F. feedback network. This means that with respect to bias the device is operated as a source follower, with the functions of the original drain and source reversed as shown in Figure 9.

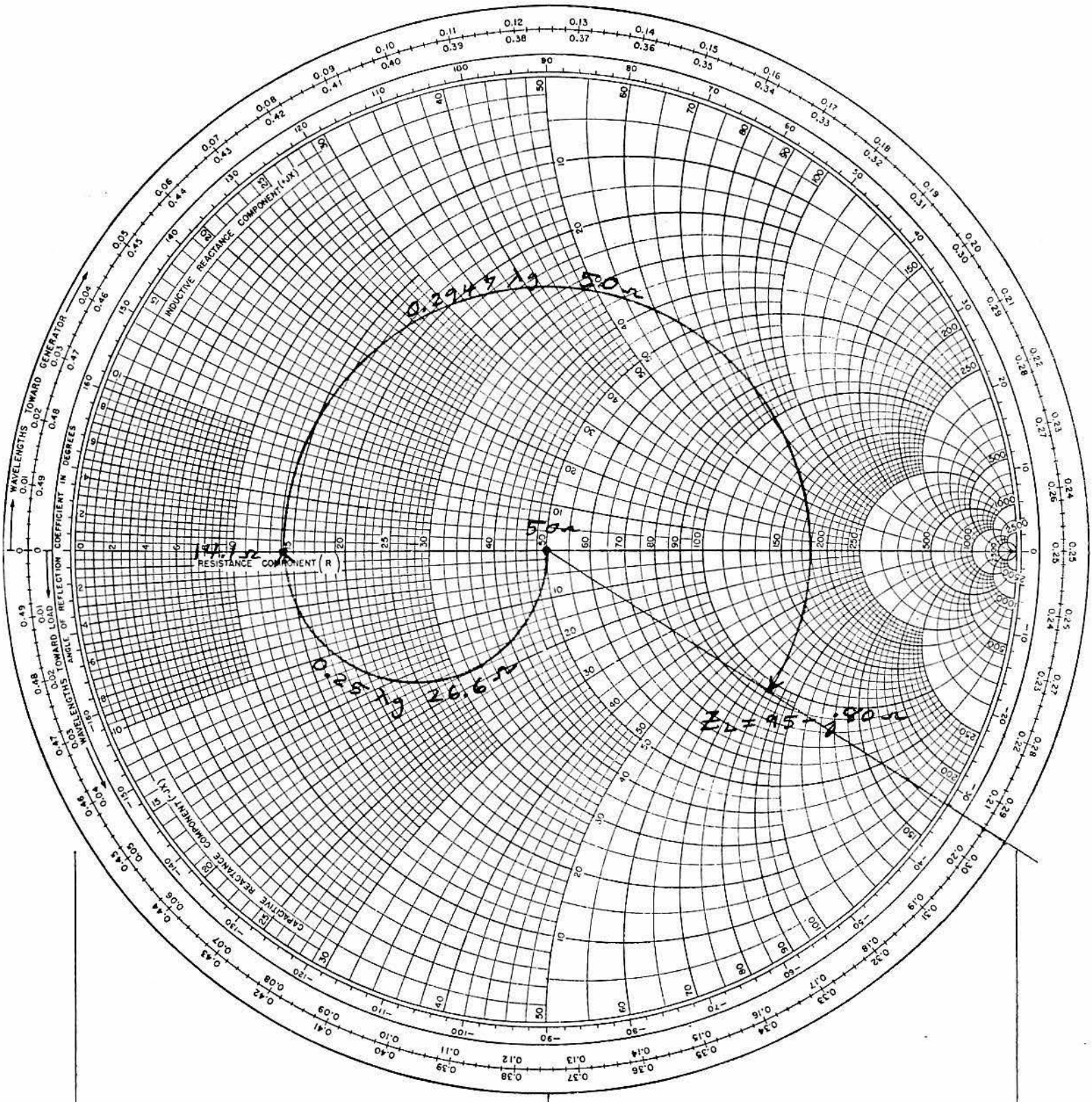
TITLE

FIGURE 3

DATE

OSCILLATOR DRAIN MATCH

IMPEDANCE COORDINATES—50-OHM CHARACTERISTIC IMPEDANCE



RADIALLY SCALED PARAMETERS

STANDING WAVE RATIO | TRANSM. LOSS: VOL. IN 1 DB STEPS | LOSS COEFF. | TOWARD GENERATOR → | ← TOWARD LOAD | REFLECTION: COEFF. | LOSS IN DB: VOL. PWR. RETN. REFL.

CENTER

Electronics - VOL. 17, NO. 1, PP-130-135, 318-325, JAN 1944

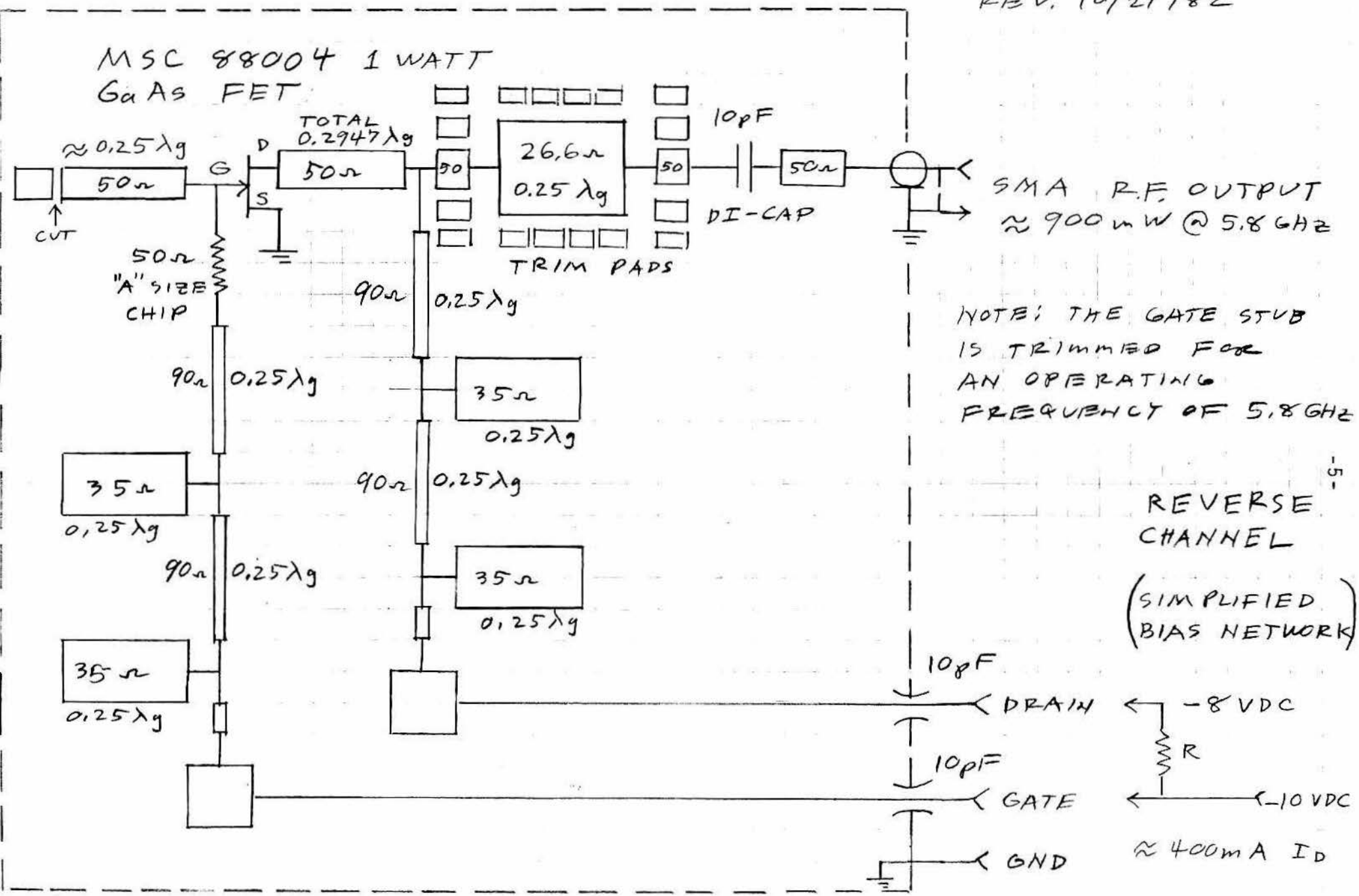
GENERAL RADIO COMPANY
WEST CONCORD, MASS.

FORM 5301-7569Z
Printed in USA

TRANSMIT OSCILLATOR SCHEMATIC

FIGURE 4

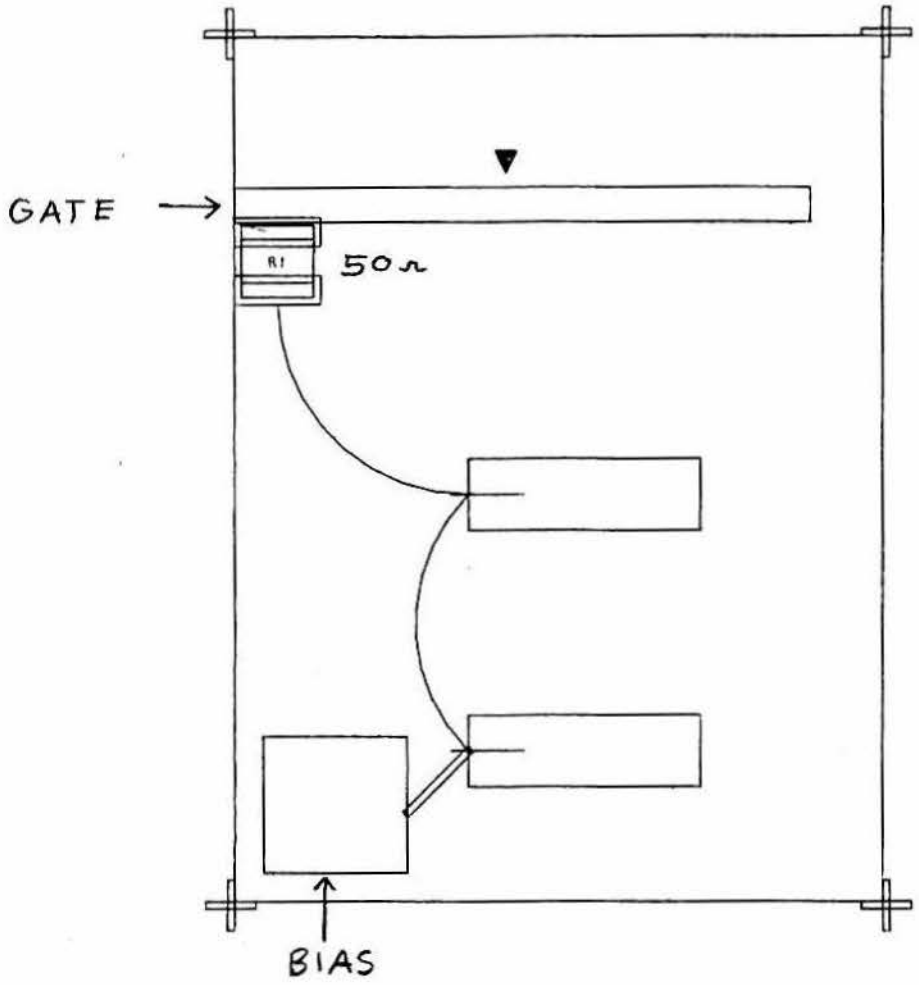
WED 8/17/82
REV. 10/21/82



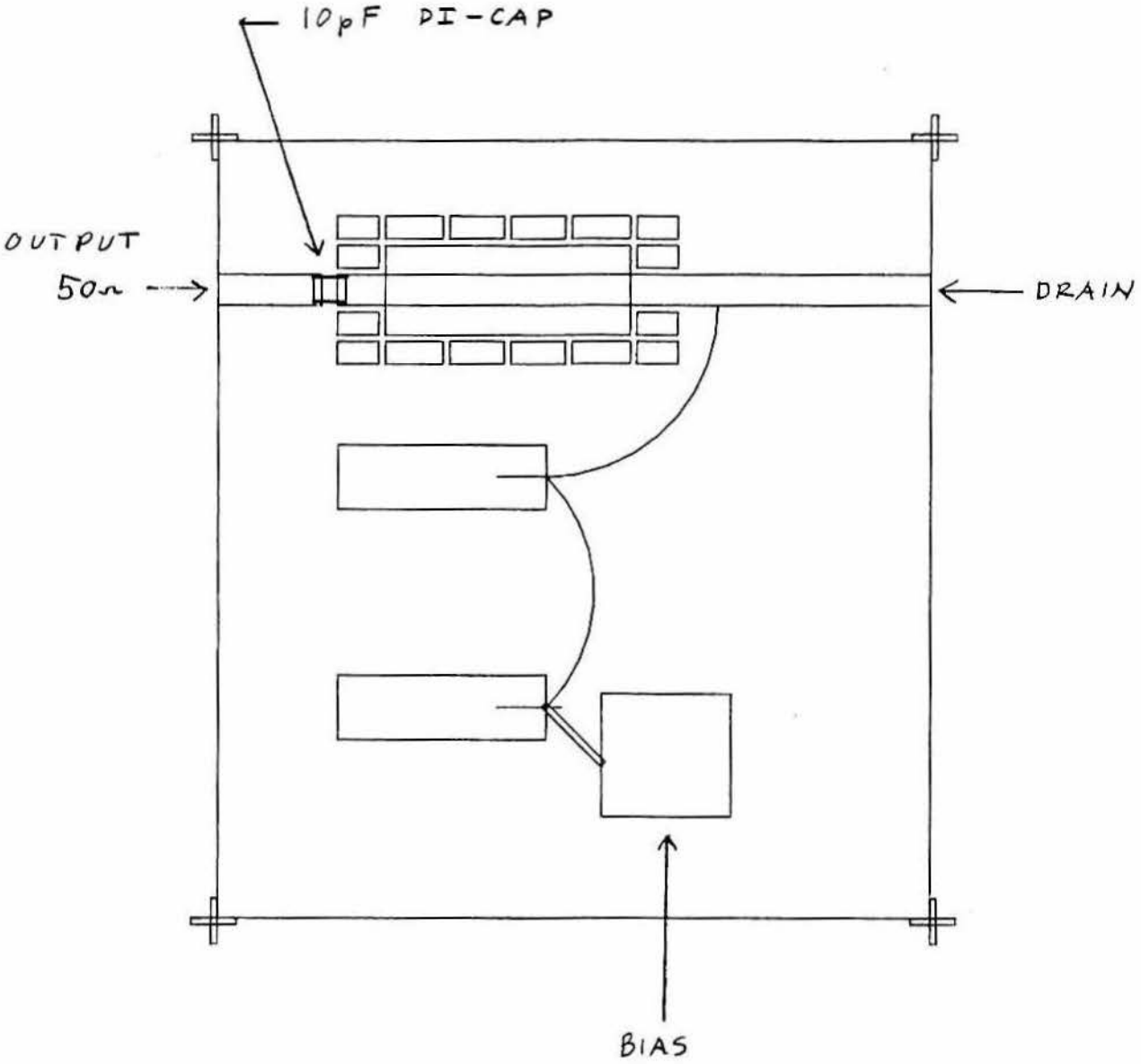
NOTE: THE GATE STUB IS TRIMMED FOR AN OPERATING FREQUENCY OF 5.8GHz

REVERSE CHANNEL

(SIMPLIFIED BIAS NETWORK)



GATE SUBSTRATE LAYOUT
Figure 5

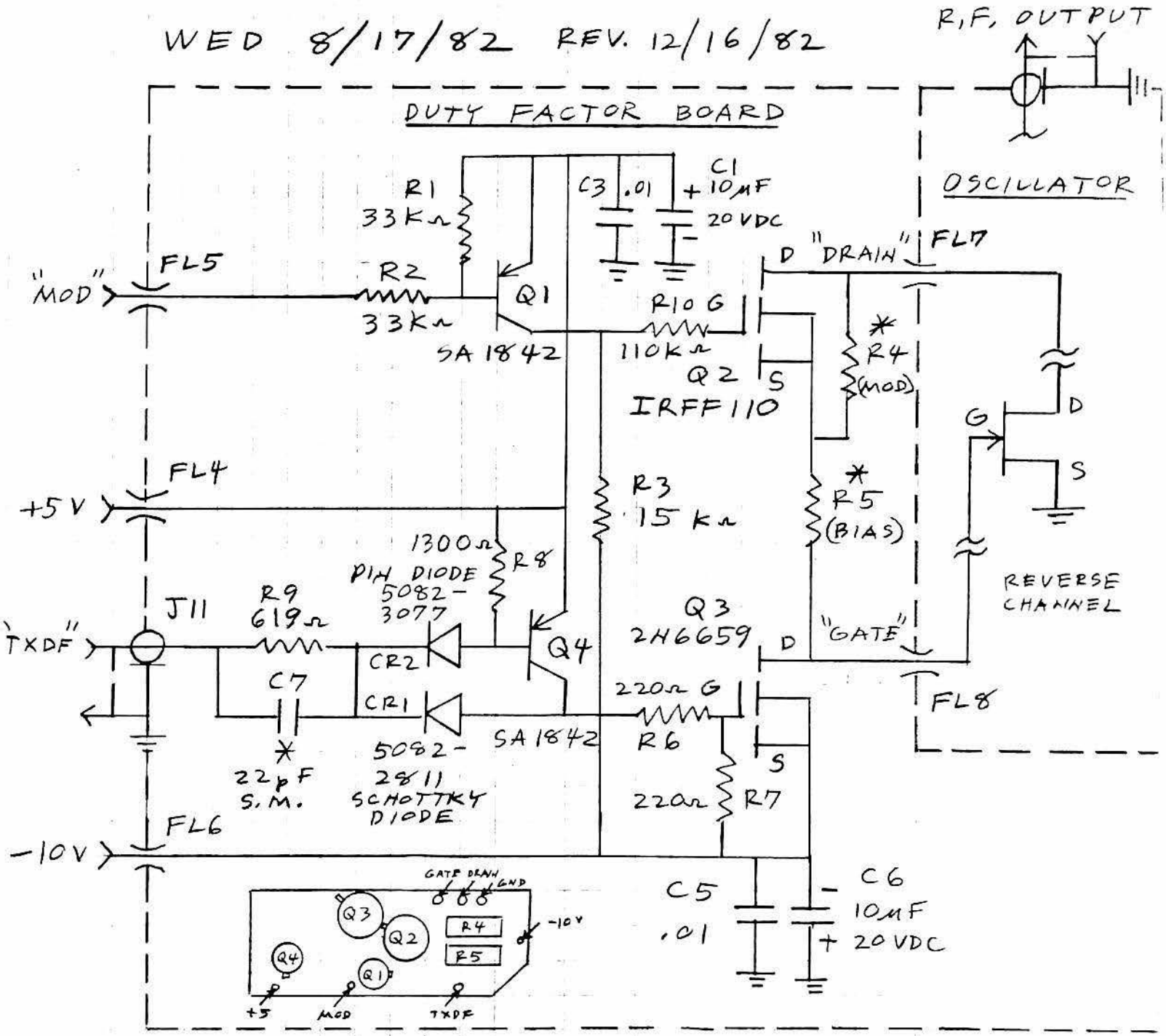


DRAIN SUBSTRATE LAYOUT

Figure 6

FIGURE 7

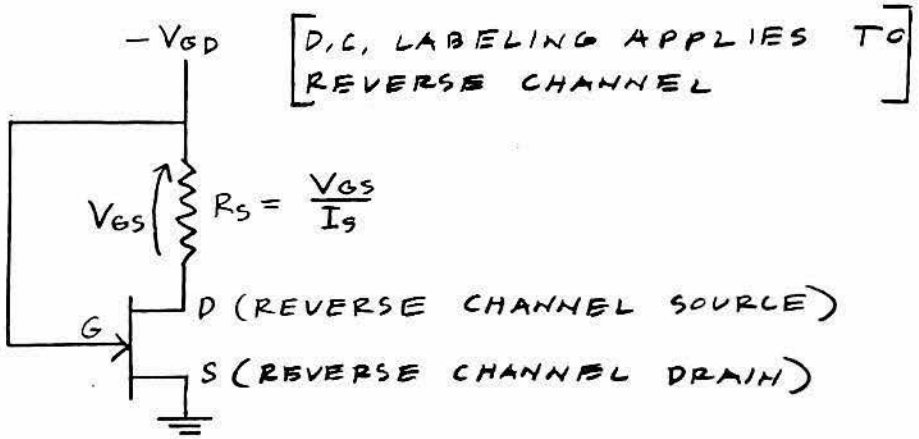
OSCILLATOR DUTY FACTOR BOARD



NOTES:

* R4 IS SELECTED FOR -1dB OUTPUT POWER WITH "MOD" LINE HIGH
* R5 IS SELECTED FOR -8VDC AT "DRAIN" WITH "XMT" LINE LOW
* C7 IS SELECTED FOR SHORTEST SWITCHING TIME AT "GATE" LINE

WED 8/23/82-2



Simplified Single Supply Reverse Channel Bias Network

Figure 8

Referring the schematic of Figure 7, the full power bias current is determined by the reverse channel source resistance comprised of R5, typical 1.78 ohms, in series with the drain to source on resistance of the VMOS modulation transistor, Q2. An IRFF110 was chosen for Q2, because of its low drain to source on resistance, typically 0.5 ohms.

To modulate the R.F. output power by -1dB, Q2 is turned off. The total reverse channel source resistance of the bias network is now increased to the sum of R4 and R5. R4 is typically set to about 5.6 ohms for a -1 dB decrease in output power.

Resistor R10 prevents damage to the internal Q2 gate to source protection zener diode with reverse bias, which may occur with the series structure of Q2 and Q3. Switching transistor Q1 provides the necessary interface to the CMOS gate at the "MOD" input. An SA1842 was chosen for Q1 based on availability.

The oscillator is gated by Q3, a 2N6659 VMOS part, chosen because of its fast switching speed as well as a low drain to resource on resistance of typically 1.6 ohms. However, it also has 50pF of input capacitance. This requires it to be driven from a low impedance source. R6 and R7 prvide this low source impedance in both the on and off drive conditions.

A bipolar switching transistor Q4 provides the necessary interface to the TTL gate at the "TXDF" input. An SA1842 switching transistor was chosen for this device based on availability and switching speed. Other faster devices could be obtained, however. If Q4 were operated into saturation, a slow turn-off time would result due to charge storage. Therefore, this device is kept in the active region by diodes CR1 and CR2, increasing switching speed. A speed-up capacitor, C7, is placed across resistor R9 to further increase switching speed.

8.1.1.4 Results

Worst case data are given for all six units over -10oC to +60oC temperature and over -9.5, -10.0, and -10.5 VDC power supply voltage at a 200ns pulse width and 20 sec period.

R5(Bias) = 1.78 ohms
R4(Mod) = 3.16 to 6.8 ohms
C7(Comp.)= 22pF

Peak full R.F. output = 28.82 to 30.37 dBm
Variation w/temp = 0.97 dB PP
Variation w/supply = 0.89 dB PP
Modulation = -0.72 to -1.69dB
Variation w/temp = 0.54 dB PP
Variation w/supply = 0.39 dB PP
D.F. Board
On delay time = 20ns to 40ns
Off delay time = 35ns to 50ns
OSC. HMC
On delay time = 20ns to 30ns
Off delay time = 10ns maximum
OSC. Assembly
On delay time = 60ns to 70ns
Off delay time = 40ns to 50ns
R.F. Frequency 5.8 GHz -71 MHz to +36 MHz
Peak Supply Current = 390mA to 753mA
Starting Voltage = 3.25 to 5.12 VDC

Note that the starting voltage for oscillation is only 5.12 VDC maximum. This indicates that the output match provides a good feedback ratio and insures fast turn-on.

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8.2.2 Video Amplifier

8.2.2.1 Description.

The video amplifier amplifies a positive going input pulse of 22mV peak to provide 600mV peak into load impedances of 25 ohms minimum. For isolation purposes the amplifier was modified to provide separate outputs for the monostatic and bistatic channels. The amplifier is used with low duty cycle pulses of minimum width 5ns at repetition frequencies of 44-81 kHz. Input impedance is a nominal 50 ohms while the output impedances are low, approximately 3 to 4 ohms. Added rise time on the bistatic output is less than 1 ns. A detector provides the input signal while the outputs supply seperate sample and hold circuits.

8.2.2.2 Design Requirements

1. Small Signal Passband Response
   Low Freq. -3 dB point << 40 KHz
   High Freq. -3 dB point $\geq$ 200 MHz

2. Gain = 600 mV peak output @ 22 mV peak input

3. Limit voltage = 800 mV

4. Limit voltage and gain stable over temperature

5. 50 ohm input impedance

6. Dual outputs - for monostatic and bistatic sample and hold circuits

7. Output impedance for each output << 25 ohms

8. No pulse amplitude compression at 650 mV peak input

9. No pulse width stretching with 650 mV peak input

10. Power supply voltages of +5 VDC and -5 VDC

11. Minimize D.C. power consumption

8.2.2.3 Design Procedure

A cutoff broadband pulse amplifier/limiter with PNP/NPN cascaded stages can be shown to minimize pulse-width stretching with increasing input signal level. Experiments showed that pulse width stretching is caused when a bipolar transistor is driven into saturation. Since a diode detector output pulse, with a low duty cycle, is always of the same polarity, the single polarity can be used to advantage in a cutoff limiter to minimize pulse width stretching. The cutoff limiter shown in Figure 1 has an additional advantage in that its simple negative feedback structure can operate satisfactorily at exceptionally high frequencies, to provide the necessary bandwidth.

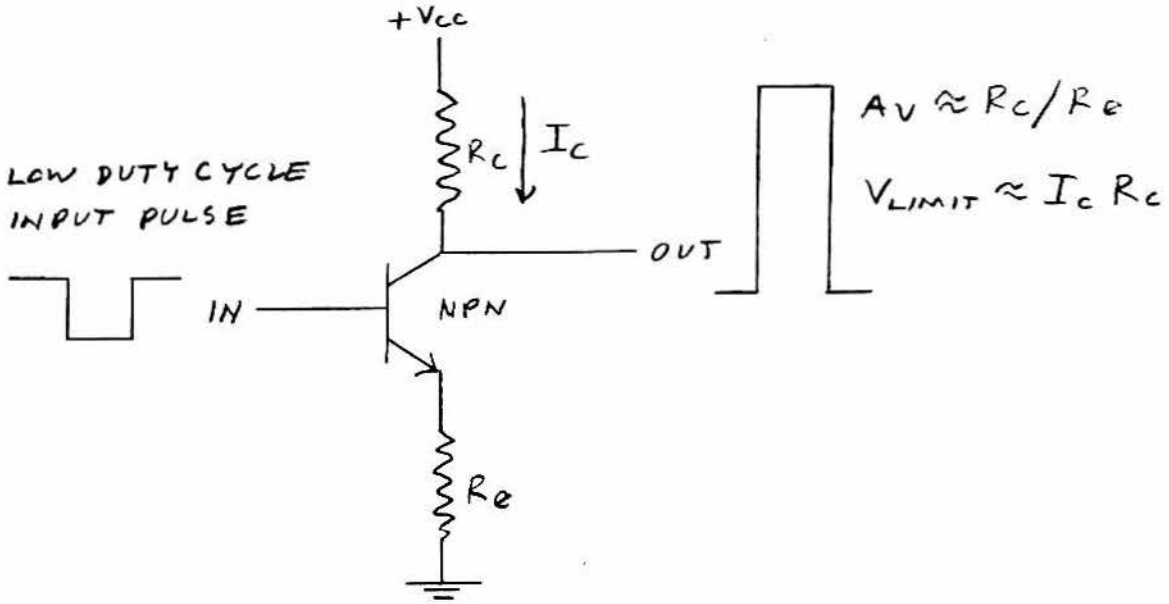


Figure 1

A negative going input pulse will drive the NPN device toward cutoff. For signal levels below cutoff the gain, Av, will be approximately the ratio of the collector resistor to the emitter resistor values, which provide negative feedback. When the device is cutoff, the collector voltage will swing from approximately $V_{cc}-I_cR_c$ to Vcc. Thus, the peak limit voltage V limit is approximately I_cR_c. Because the device is always being driven toward cutoff, pulse stretching is minimized. Experimentally it was determined that Re must be $\geq$50 ohms to provide a reasonable approximation to the Rc/Re voltage gain. This was probably due to device parasitic emitter resistance.

If a positive input pulse is required to produce a positive going output pulse, cascades of PNP/NPN stages can be used as shown in Figure 2. In this configuration, each stage will always be driven toward cutoff minimizing pulse width stretching with increasing input signal level.

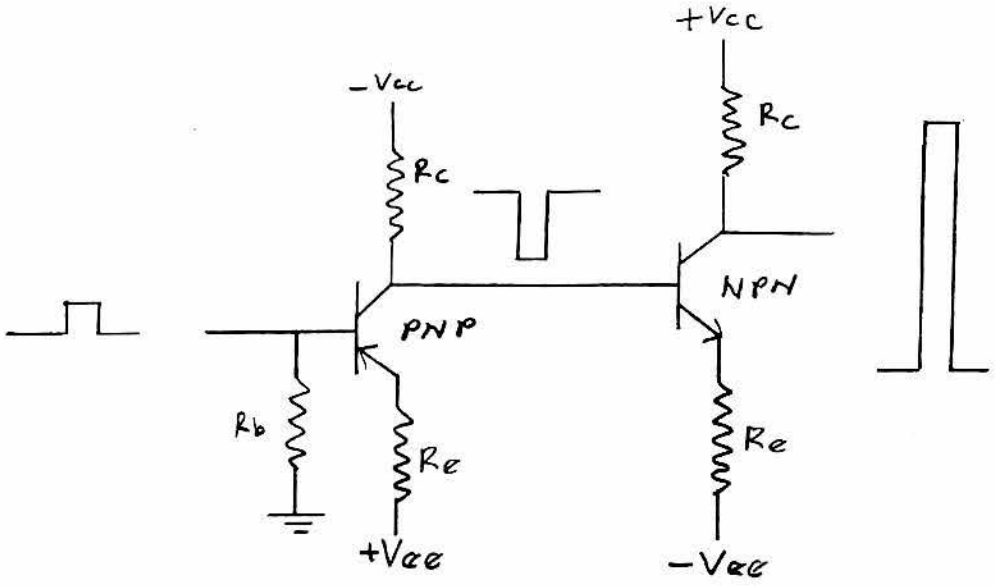


Figure 2

For temperature stability and circuit simplicity, an AC coupled conventional dual bias scheme can be utilized as shown in Figure 3. If Vee>> Vbe and if the device hfe is high, then the collector current will be stable with temperature relative to V_{be} variations. Therefore gain and limit voltages will be stable with temperature.

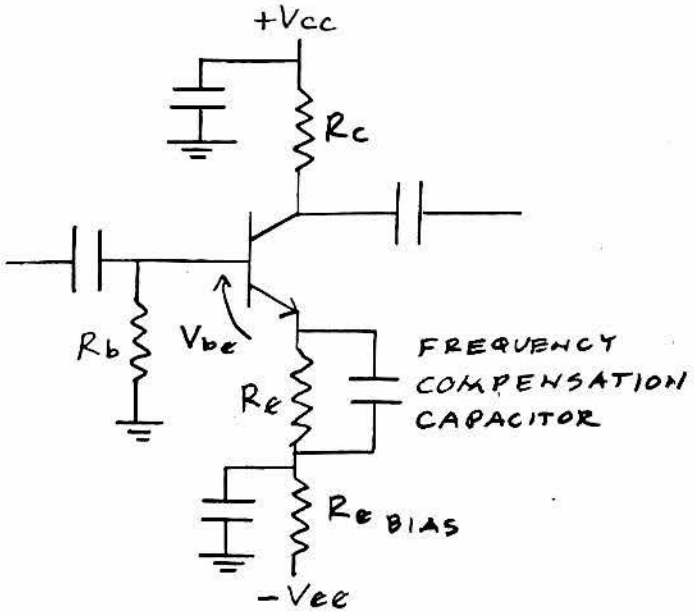


Figure 3

Frequency compensation can be accomplished by selecting chip capacitors placed acoss each emitter resistor. Emitter resistor inductance was minimized by using chip components to maximize bandwidth and prevent spurious oscillations. Re must be kept > 50 ohms to minimize transistor parasitic emitter resistance effects, but the collector resistance must be kept small to minimize rise time effects in cutoff. Re = 50 ohms and Rc_{total} = 150 ohms provided a suitable compromise for this bandwidth.

To achieve the required low frequency response as well as a good high frequency response, 1 microFarad chip capacitors were used for both bypassing and coupling.

Emitter followers were added to the last stage to provide low output impedances and isolation betwen outputs. The resultant output impedance should be approximately equal to the input impedance divided by the beta of the device. In practice, however, this appears limited to about 3 ohms, probably a result of parasitic emitter resistance.

The complete circuit is shown in Figure 4. R22 provides 400µA of DC bias to the positive polarity diode detector to obtain maximum detector sensitivity. R1 provides the appropriate terminating impedance for the diode to video amplifier coaxial cable.

The positive polarity low duty cycle pulse at 22 mV peak voltage drives the first PNP/NPN pair Q1 and Q2. Each individual gain stage provides approximately a voltage gain of 2.3 resulting in a total output voltage of 600 mV peak for four stages under linear conditions.

A base return resistor was added to each stage because of the AC coupling to provide a ground reference bias for each following base. The value was chosen equal to that of each collector resistor to provide acceptable pulse recovery. Thus, the effective collector resistance is equal to one-half the collector resistor value. This also divides the limit voltage by two as shown in Figure 5.

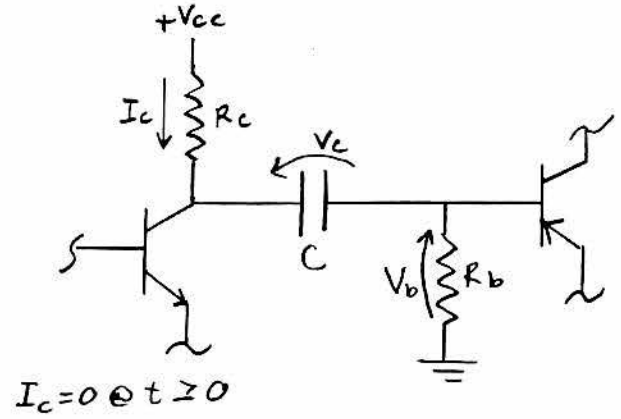
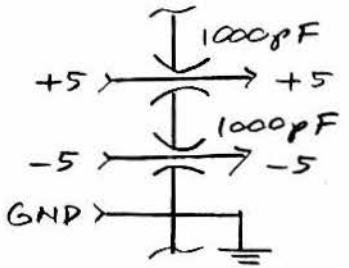


Figure 5

VIDEO AMPLIFIER (DUAL OUTPUT)

W. E. DUMKE 11/5/82 REVISED 11/8/82



NOTES: - ⊂⊃ 15 FERRITE BEAD

- R1, R3, R7, R11, R16, R18, R23 ARE CHIP RESISTORS
- (*) SELECTED VALUES

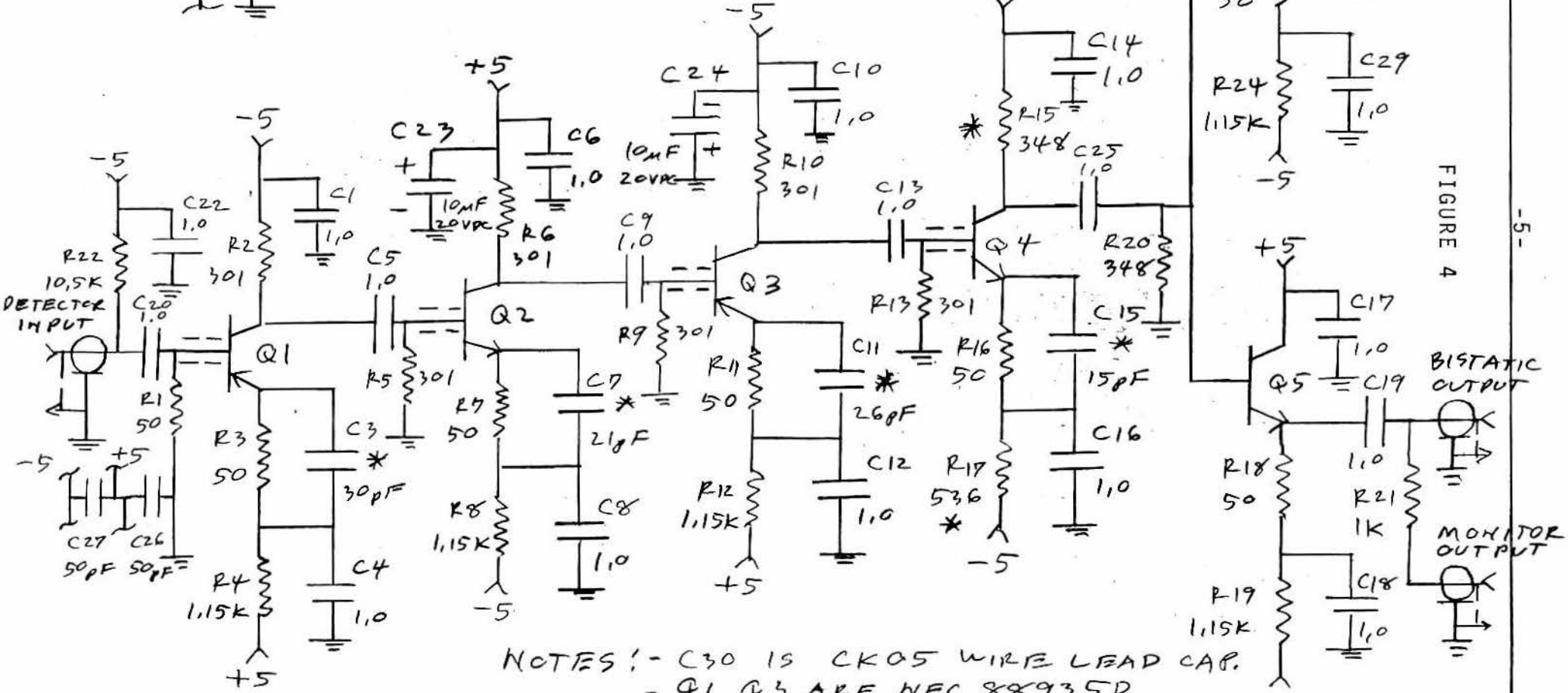


FIGURE 4

NOTES: - C30 IS CK05 WIRE LEAD CAP.
- Q1, Q3 ARE NEC 88935D
- Q2, Q4, Q5, Q6 ARE NEC 02107
- C20 IS ISOLATED FROM BIAS LINES BY KAPTON SHEET.
- C29 IS ISOLATED FROM C18 BY KAPTON SHEET

Assume at time $t < 0$, the base current of the following stage is negligible. Then $V_c = V_{cc} - I_cR_c$ and $V_b = 0$. If at time $t = 0$, the first transistor is cutoff, then $I_c = 0$. The charge on the capacitor cannot change instantaneously. Therefore, the pulse amplitude seen at V_b will be:

$$V_b(t=0) = [V_{cc}-(V_{cc}-I_cR_c)[R_b/(R_b + R_c)]$$

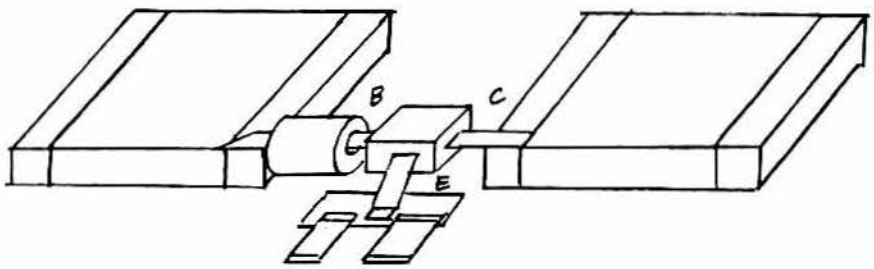
If $R_b = R_c$, then $V_b(t=0) = (1/2)\ (I_cR_c)$.

In the actual circuit, the limit voltage was chosen to be 800 mV peak.

The two 10 microfarad tantalum capacitors were added to prevent logic noise from coupling into the video amplifier, and resistor R21 was added to provide coupling for an oscilloscope monitor line on the output.

Good layout is very critical for this wide bandwidth circuit. The most critical parasitic is the emitter inductance from each device's case to the emitter RC networks. A short-fat structure is highly desirable to minimize series inductance. Because of the very low output impedance of the emitter followers, the line from each emitter to each output connector must be kept as short as possible. The collector leads are less critical, since series inductance will tend to aid the high frequency response. Bias lines after bypassing are the least critical, after care is taken to minimize possible RF feedback paths in the microwave region. The assembly drawing is shown in Figure 6.

Spurious regeneration modes at 2.5 GHz due to stray capacitances from the transistor packages to the ground plane were eliminated by lifting the transistors from the surface of the P.C. board, and placing ferrite beads on each device base as shown in Figure 5.



Modified Transistor Mounting
Figure 5

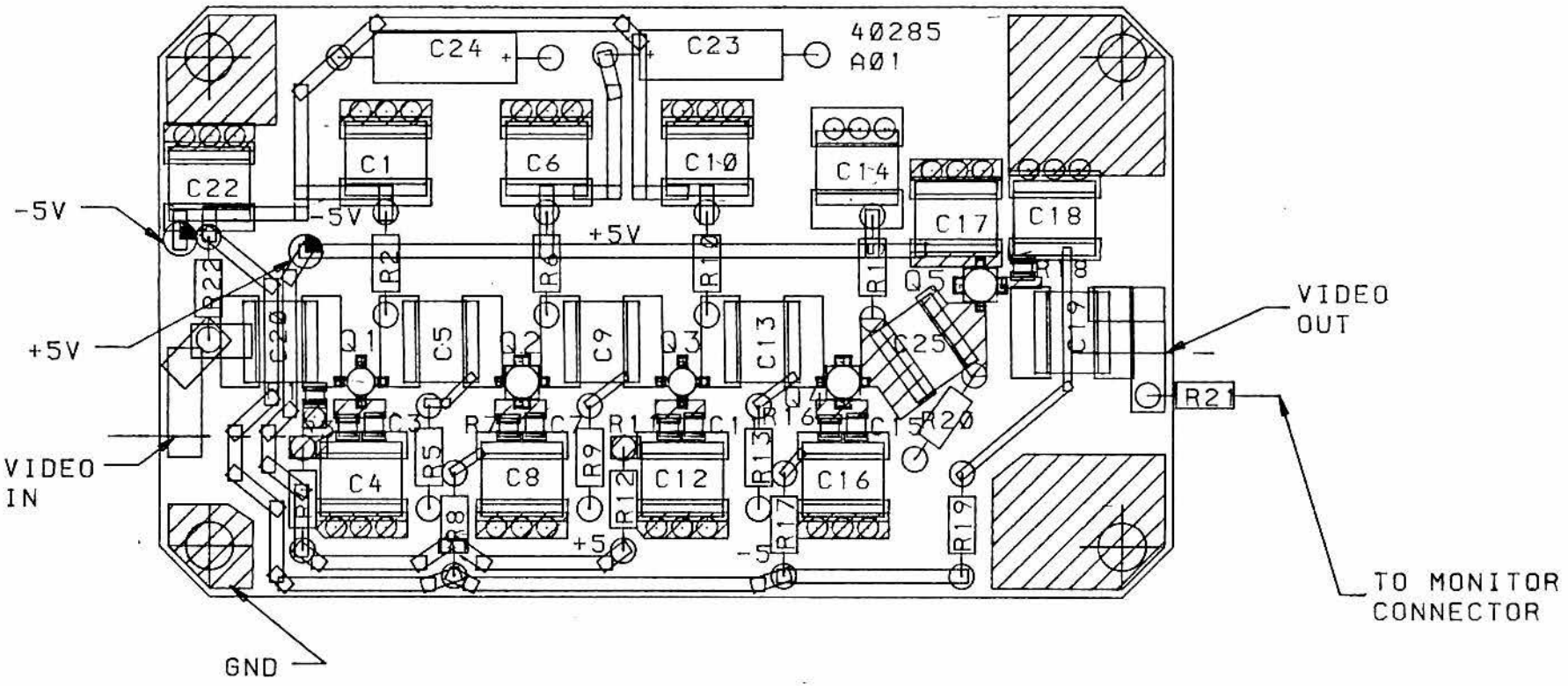

40285
A01
C24
C23
C22
C1
C6
C10
C14
C17
C18
C19
C20
C25
R2
R6
R10
R14
R18
R21
R22
Q1
Q2
Q3
Q4
Q5
-5V
+5V
VIDEO
IN
VIDEO
OUT
GND
TO MONITOR
CONNECTOR

Figure 6

8.2.2.4 Results

Because of schedule limitations, measurements on only serial numbers 101, 105 and 106 were completed after the additional emitter follower output was added. Worst case values over temperature for all of these three units are presented. A data summary of worst case values for the units previously tested with only a single output, S/N 101, 102, 103 and 104 is also presented for comparison.

	S/N 101/105/106 MONOSTATIC OUTPUT	S/N 101/105/106 BISTATIC OUTPUT	S/N 101/102/103/104 SINGLE OUTPUT
Idc @ +5 VDC	(24.0 mA to 25.1 mA)		(20.5 mA to 21.8 mA)
Idc @ -5 VDC	(24.6 mA to 25.7 mA)		(20.5 mA to 22.3 mA)
Rout @ 25 ohms	3.0 ohms	2.6 ohms	3.6 ohms
Gain @ 25 ohms	0.5 dBpp	0.4 dBpp	0.6 dBpp
Limit Voltage @ 25 ohms	1.3 dBpp	1.1 dBpp	0.8 dBpp
Added Rise Time @ 22mV Input	1.2 nS	0.9 nS	0.6 nS
Added Rise Time @ 650mV Input	2.4 nS	2.1 nS	1.8 nS
Pulse Stretching	1.2 nS	1.4 nS	1.2 nS
Added Fall Time @ 22mV Input	0.3 nS	0.1 nS	$\leq \lvert -0.2\text{nS} \rvert$
Added Fall Time @ 650mV Input	$\leq \lvert -0.3\text{nS} \rvert$	$\leq \lvert -0.4\text{nS} \rvert$	$\leq \lvert -0.5\text{nS} \rvert$
Small Signal Low frequency -3dB cutoff	App. 5 KHz	App. 5 KHz	App. 5 KHz
Small Signal High frequency -3dB cutoff	286 MHz	364 MHz	430 MHz

Photographs of the bistatic output waveforms and passband response are given below for video amplifier S/N 106. Because of the limited rise and fall times of the pulse generator source, photographs of its waveforms are presented for comparison.

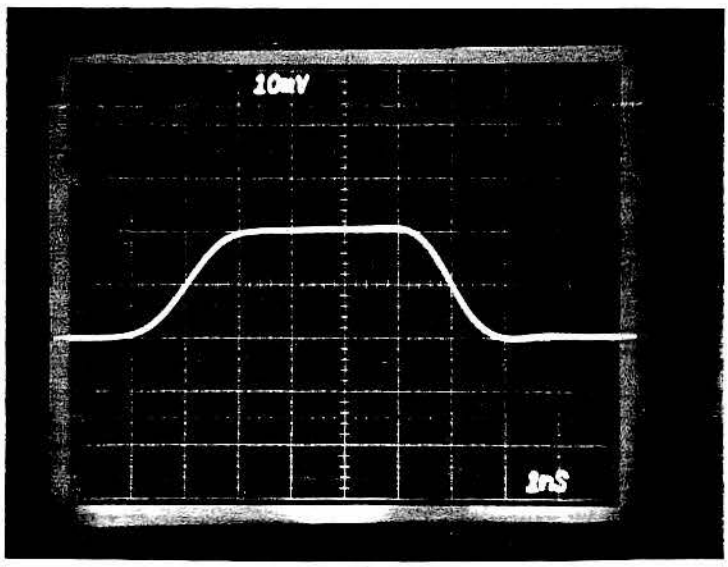


Figure 7
Pulse Generator Output @ 22mV Peak

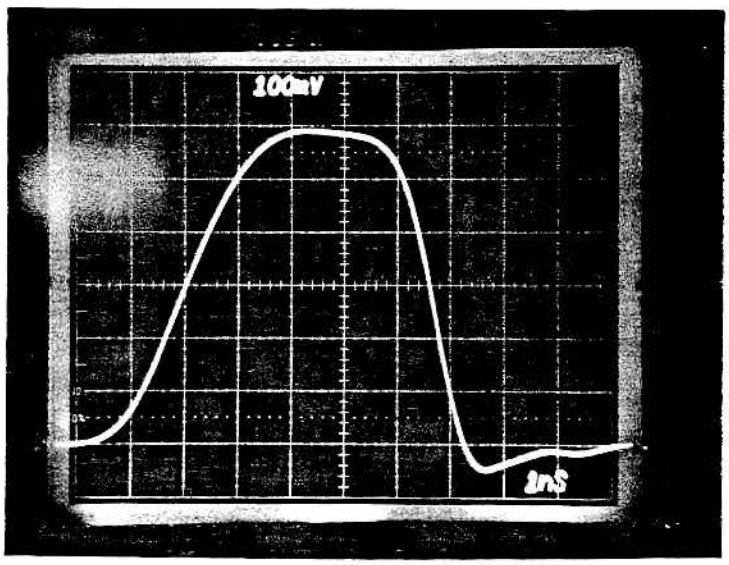


Figure 8
Video Amlifier Bistatic Output at 22mV Peak Input

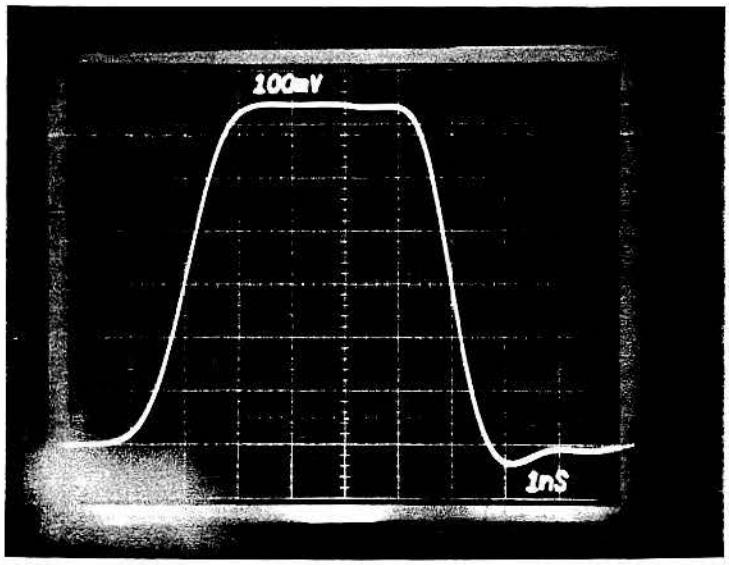


Figure 9
Pulse generator Output
@ 650 mV Peak

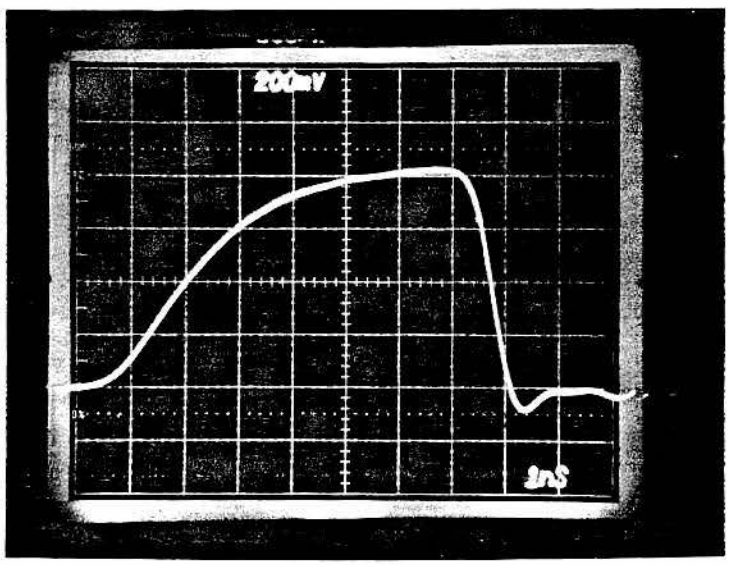


Figure 10
Video Amplifier Bistatic
Output at 650mV Peak
Input

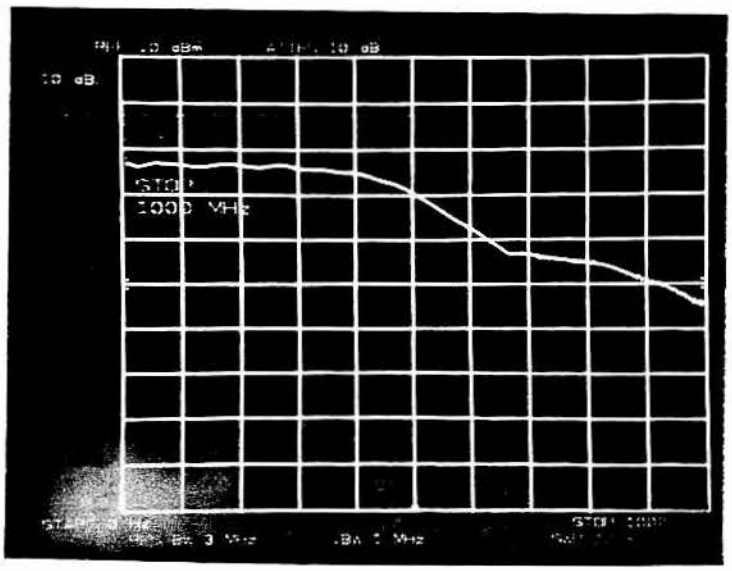


Figure 11
Video Amplifier Bistatic Output Small Signal Passband Response at -40dBm Input

Note that the rise time of the output waveform increased significantly when the amplifier was driven into limit. In the linear region the rise time is dependent on the frequency compensated response of the amplifier. When the amplifier is driven into cutoff, the frequency compensation no longer functions and the rise time is therefore slower. However, when the input pulse is removed, the transistors switch from cutoff to the active region. Therefore the fall time is frequency compensated and is approximately the same as the fall time in the small signal condition.

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